Peripheral Power Controller for Pentium® 4 Computer Systems (HIP6521EVAL1)

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Introduction

The progress of the advanced computing cores coming from microprocessor manufacturers such as Intel and AMD have necessitated a change in the topology of the switching regulators traditionally used to power these processor cores. Multiphase buck regulators have proven to be the topology of choice for such high-current applications. However, the distributed power system architecture of these computers continue to have a need for other sub-system specific voltages. The HIP6521 was created to complement a multiphase buck controller in creating a complete power solution for the typical Pentium 4 system. Athlon-class processor based systems (AMD) may also benefit from the HIP6521. [1]

The HIP6521EVAL1 evaluation board embodies a 4-output regulator solution targeted at supplying power to the system memory (2.5V), system clock (2.5V), ICH/MCH chip set core (1.8V), and the 4X AGP video (1.5V), with provisions for ACPI power management implementation. [2]

Quick Start Evaluation

Important!

To facilitate the evaluation of the HIP6521 in a typical setting, the HIP6521EVAL1 was designed to be powered primarily from an ATX supply. However, the board does have hook-up turret terminals that allow it to be piggy-backed in an actual computer system, or be powered from standard laboratory power supplies

If an ATX power supply is used to power the board (using the on-board 20-pin connector), remember that regulation of most ATX supplies is generally dependent on the presence of a DC load on the main 5V output. Therefore, for best results, have a 5Ω/25W-50W power resistor connected to the 5V output of the ATX supply (take necessary precautions, as the resistor may get very hot). [3]

Circuit Setup

Before connecting an input supply to the board, consult the circuit schematic and familiarize yourself with the various connection options offered by the HIP6521EVAL1.

➤ Set Switches

Ensure the ‘ATX ON’ (**SW1**) switch is in the off position (away from ‘ATX ON’ marking) and ‘S3/S5’ (**SW2**) switch is in the middle position (away from ‘S3’ or ‘S5’ marking).

SW3 helps with the control of the various outputs in ACPI shutdown states. To avoid having the powerful output drives (of the regulators that have to be off in certain sleep states) hold the outputs within regulation, they have to be actively kept off by pulling the corresponding FB pins above 1.25V.

Each output can thus be turned off or kept running in S3 and/or S5 states, with corresponding consequences. For initial evaluation, we recommend closing positions 2, 4, and 6-8 (see Figure 1 for detail). Unless otherwise specified, this recommended SW3 configuration was employed throughout testing of the board described in this application note.

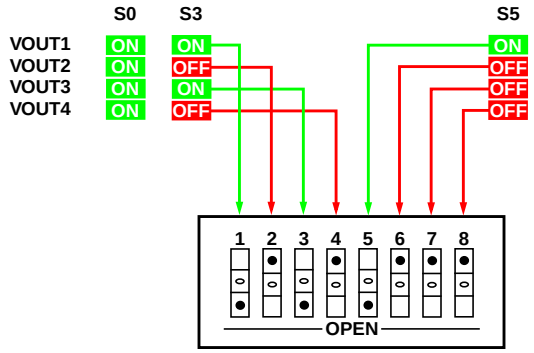


FIGURE 1. SW3 DETAIL (RECOMMENDED INITIAL CONFIGURATION) - SLEEP STATES SUPPORT

➤ Set Jumpers JP1-4

JP1 and JP3 select the on-board input voltage for the linear pass elements corresponding to the VOUT3 and VOUT4 outputs, respectively. One recommended configuration for initial evaluation is with JP1 populated in the ‘2.5VIN’ position and JP3 in the ‘3.3VIN’ position.

JP2 and JP4 select the ‘+3.3VDUAL’ as the input for the two linear pass elements mentioned above. If an external 3.3VDUAL source is supplied, either pass element (Q4 and/or Q5) may be powered from this source by moving the respective header jumper from JP1 or JP3, onto JP2 or JP4, respectively.

➤ Hookup Guide Using Standard Bench Supplies

Connect a 5V, 16A supply to the +5VDUAL input and a 3.3V, 4A, supply to the +3.3VIN input. Another 3.3V, 4A supply may be needed for the optional +3.3VDUAL input if either JP2 or JP4 are populated. Connect typical loads to all the evaluation board’s outputs. Consult Table 1 for maximum loads supported by the design of the in the configuration received; consult the ‘Modifications’ section for information on modifying the evaluation board to meet your special needs.

➤ Hookup Guide Using a Standard ATX Supply

Connect the 20-pin ATX connector to the on-board J1 mating connector. Connect typical loads to all the evaluation board’s outputs. Consult Table 1 for maximum loads supported by the design of the in the configuration received; consult the ‘Modifications’ section for information on modifying the evaluation board to meet your special needs.

➤ **Hookup Guide for Piggy-Backing the Evaluation Board Into Your System**

Connect GND, +5VDUAL, +3.3VIN, and +3.3VDUAL turret terminals to the corresponding voltages present on your system board. For ACPI functionality, connect $\overline{S3}$ IN (TP9) and $\overline{S5}$ IN (TP10) to your system's $\overline{S3}$ and $\overline{S5}$ signal source. Connect the evaluation board's outputs to the corresponding power planes in your system. Consult Table 1 for maximum loads supported by the design of the in the configuration received; consult the 'Modifications' section for information on modifying the evaluation board to meet your special needs.

Operation

➤ **Provide Power to the Board**

Turn on the bench supplies or the system onto which the board is piggy-backed.

If using an ATX supply, plug it into the mains. If the supply has an AC switch, turn it on. The '5VSB', '5VDUAL', and 'S0' LEDs should light up, indicating the presence of 5V standby and 5V dual voltages on board, as well as indicating active state selection. Flip on the 'ATX ON' switch and shortly thereafter '5VIN' and 'ATX PGOOD' LEDs should light up indicating the presence of main ATX 5V on board, as well as the ATX PGOOD indication.

➤ **Examine Start-Up Waveforms / Output Quality Under Varying Loads**

Start-up is immediate following application of bias voltage. Using an oscilloscope or other laboratory equipment, you may study the ramp-up and/or regulation of the controlled voltages.

In either state (active or S3, S5) vary the output loads to simulate computer loads typical of the specific operating state the circuit is in. Observe the limitations of the circuit while in S3 or S5 states: all output power, along with any necessary operating bias current, is delivered from the ATX supply's 5VSB output.

➤ **Examine State Transitions**

For subsequent transitions into/out of standby states, leave the main ATX outputs enabled (SW1 on); the on-board circuitry will automatically turn them off when entering a standby state and re-enable them when transitioning back into active state. To enter a standby state, flip SW2 to the position indicating the desired standby state. The 'S3' LED lights up to indicate S3 standby state, while S5 state is indicated by illumination of the 'S5' LED. Active state indication is performed by the 'S0' LED.

Fault Handling

In case of a fault condition (output under-voltage on the linear outputs, or overcurrent on the switching output), the faulting output shuts down and undergoes an individual re-start attempt every 3 soft-start (SS) intervals. Review the appropriate data sheet section for more detail.

Reference Design

General

The evaluation board is built on 1-ounce, 4-layer, printed circuit board (see last three pages of this application note for layout plots). Most of the components specific to the evaluation board alone, which are not needed in a real computer application, are placed on the bottom side of the board. Left on top of the evaluation board are the components necessary to exemplify a typical application, as well as the user interface (input/output terminals, test points, switches, etc.).

Design Envelope

Although a real-life computer system application might have different requirements, the HIP6521EVAL1 board was designed to meet the maximum output loading described in Table 1. Note the fact that the sleep state output currents are likely limited only by the ATX power supply's 5VSB output capability. As all the outputs operate the same current paths in both active and standby states, standby state power dissipation capability equals that of active state. Dynamic output tolerances and current ratings can be adjusted by properly selecting the components external to the HIP6521.

TABLE 1. HIP6521EVAL1 MAXIMUM OUTPUT LOADING

OUTPUT VOLTAGE	ACTIVE STATE		SLEEP STATES		TOL. (STATIC/ DYNAMIC)
	I_{OUT}	dI_{OUT}/dt	I_{OUT}	dI_{OUT}/dt	
2.5VMEM	8.0A(pk) 3.0A(avg)	1A/µs	0.2A (Note)	0.1A/µs (Note)	3%/5%
2.5VCLK	1.0A(pk) 0.4A(avg)	0.1A/µs	OFF	OFF	5%/5%
1.8VMCH	3.0A(pk) 1.0A(avg)	1A/µs	0.1A	0.1A/µs	5%/5%
1.5VAGP	3.0A(pk) 0.8A(avg)	1A/µs	OFF	OFF	5%/5%

NOTE: In real applications, this output is OFF in S4/S5; requires 1.8VMCH to derive power from the 3.3VDUAL supply (not provided on the HIP6521EVAL1).

From a thermal performance perspective, do not operate the evaluation board for extended periods of time at output current levels exceeding the design envelope, as detailed in Table 1.

Performance

Figures 2 through 8 depict the evaluation board's performance during typical operational situations. To simulate minimum loading conditions, unless otherwise specified, the outputs were loaded with 65Ω resistive loads.

Soft-Start Start-Up

Figure 2 shows a typical HIP6521EVAL1 start-up. For this capture, the ATX supply powering the board is turned on, at time T0, with SW1 on and SW2 is in the S0 (middle) position. At time T1 the input supply exceeds the power-on-reset (POR) threshold and the 2.5VMEM and 1.8VMCH outputs start ramping up toward their target value, which

they reach at time T2. Between T1 and T2, due to the fact the ATX 3.3V output has not come up already, the 2.5VCLK and 1.5VAGP outputs experience an under-voltage event which keeps them off for a period of three soft-start cycles. At time T3, the main ATX outputs start to ramp up. Time T4 signals the beginning of the 2.5VCLK and 1.5VAGP soft starts, with the outputs reaching their set point at time T5.

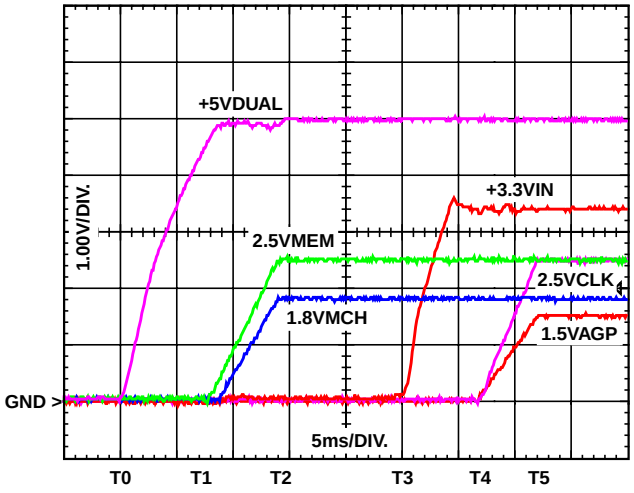


FIGURE 2. HIP6521EVAL1 START-UP

Active to Standby State Transition (S0 -> S3)

Figure 3 shows a typical active (S0) to S3 standby state transition. Prior to time T0, the HIP6521EVAL1 was operating in active state. At time T0, SW2 is switched into the 'S3' position. As a result, the main ATX outputs, as well as the 2.5VCLK and 1.5VAGP outputs are shut down. Even though the ATX is effectively shut down at time T0, the ATX PGOOD output signals the fact that the main outputs will go out of regulation only at time T1. At time T2, the ATX 3.3V outputs start to discharge, falling out of regulation. Throughout the transition, the 2.5VMEM and 1.8VMCH outputs rigorously maintain their regulation.

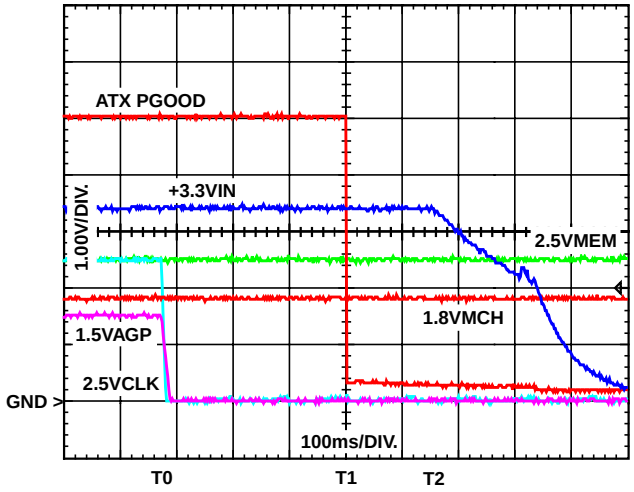


FIGURE 3. ACTIVE TO S3 STANDBY STATE TRANSITION

Standby to Active State Transition (S3 -> S0)

Figure 4 shows the reversal of the process described in Figure 3. By flipping SW2 back to the S0 (middle) position at time T0, the ATX supply's main outputs are enabled, along with the HIP6521-controlled 2.5VCLK and 1.5VAGP outputs. Time T1 signals the return of the ATX PGOOD signal back to a high state. Noteworthy is the lack of perturbations in the 2.5VMEM and 1.8VMCH outputs during this state transition.

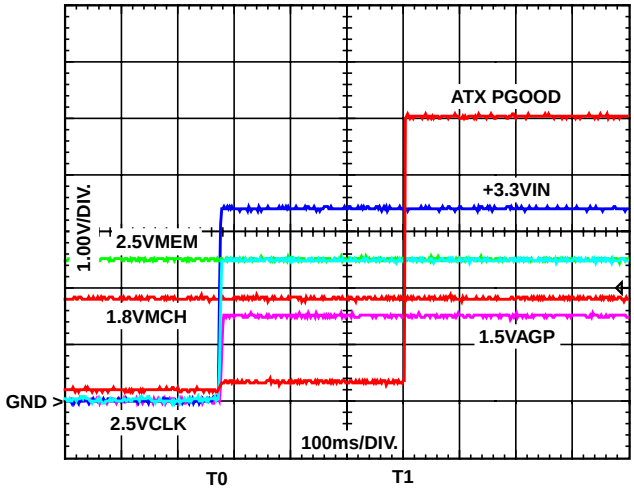


FIGURE 4. S3 STANDBY TO ACTIVE STATE TRANSITION

Due to the similar transition response, only S3 state transitions are detailed.

Transient Response

Figure 5 details the transient response of all four outputs controlled by the HIP6521 under the effect of concurrent loading. The characteristics of the loads the outputs were subject to during this test are listed in Table 2. To summarize the information, all outputs were transiently loaded with 10% to 100% of their maximum output rating, under nominal current rate of change, a 40% duty cycle, and different frequencies resulting in random load overlapping. The test was designed to stress the application in a manner representative of a worst-case situation. Even under such loading, the HIP6521EVAL1 exhibits exemplary response and crosstalk immunity, both characteristics easily noticed in Figure 5.

TABLE 2. OUTPUT TRANSIENT LOADING DESCRIPTION

OUTPUT	$I_{OUT(MIN)}$ (A)	$I_{OUT(MAX)}$ (A)	dI_{OUT}/dt (A/µs)	Frequency (Hz)
2.5VMEM	0.8	8.0	1.0	1000
2.5VCLK	0.1	1.0	0.1	800
1.8VMCH	0.3	3.0	1.0	650
1.5VAGP	0.3	3.0	1.0	1500

NOTE: All transients applied had a 40% duty cycle.

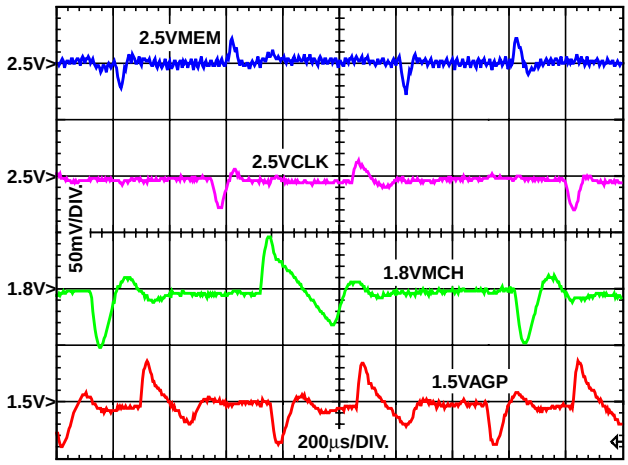


FIGURE 5. OUTPUT TRANSIENT RESPONSE (CONCURRENT LOADING OF ALL OUTPUTS)

Output Short-Circuit Protection

In response to an over-current event on the switcher's output, or an under-voltage event on any of the linear outputs, the faulting regulator is shut down. Figure 6 exemplifies such a scenario on 1.5VAGP (VOUT4). At time T0, a short-circuit is applied to the 1.5VAGP output; as a result, the output and the ATX 3.3V input start to sag under the increasing output current. DRIVE4 responds by increasing the base drive for the pass element (Q5). At time T1, DRIVE4 reaches its output current limit. The ATX 3.3V output reflects the current limit event through the settling of the voltage seen between times T1 and T2. As the current drawn in current limiting from the ATX supply does not equal the output current drawn by the short-circuit, the 1.5VAGP output continues to drop. At time T2, the 70% undervoltage threshold is reached and the output is shut down.

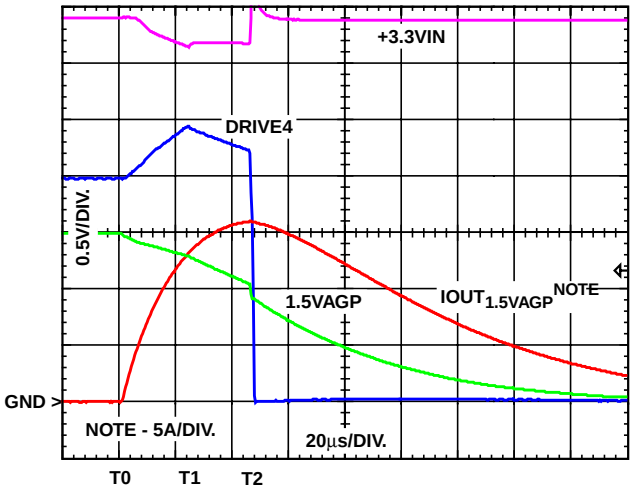


FIGURE 6. HIP6521EVAL1 VOUT4 UNDER-VOLTAGE RESPONSE (SHORT-CIRCUIT PROTECTION)

Following an over-current shutdown, a restart attempt is performed after approximately 3 soft-start periods. Figure 7 zooms out of the picture presented in Figure 6 in order to detail the restart attempt under a continuous output short-circuit. Time T0 marks the application of the output short-circuit. At time T1, after approximately 3 soft-start intervals, DRIVE4 attempts to restart the output: the output voltage, and, consequently, the output current ramp up. As the output current ramps up, the DRIVE4 pin enters current limiting, and 25% into the SS ramp under-voltage monitoring is enabled. At time T2 the fault condition is detected and the output is shut down. The cycle repeats for as long as the short-circuit is present at the output.

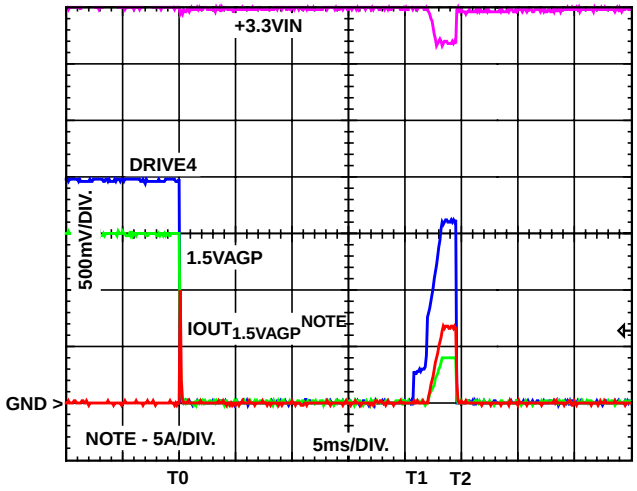


FIGURE 7. HIP6521EVAL1 VOUT4 HICCUP MODE UNDER APPLIED SHORT CIRCUIT

Switching Regulator Efficiency

Figure 8 highlights the evaluation board's conversion efficiency with only the switching section loaded. The measurement was performed at room temperature with the linear outputs open and 100 LFM of air flow.

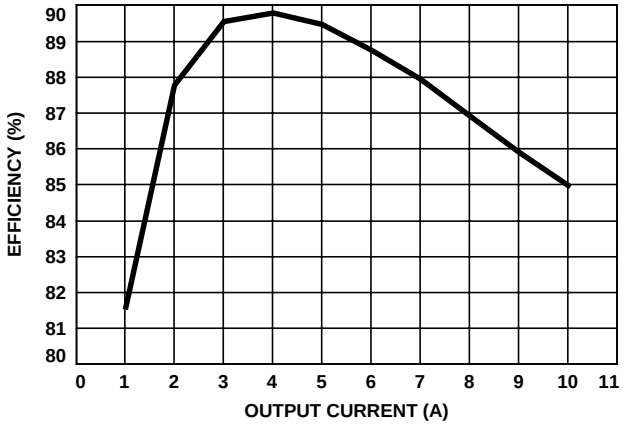


FIGURE 8. HIP6521EVAL1 SWITCHING REGULATOR MEASURED EFFICIENCY (ALL LINEAR OUTPUTS UNLOADED)

Modifications

Adjusting the Output Voltage

All outputs controlled by the HIP6521 are adjustable by means of the resistive divider connecting the FB pins to their respective outputs.

The switching regulator's output has provisions for droop implementation, unused in the shipping configuration. As R8's value plays in the feedback compensation, it is recommended VOUT1 is adjusted by adjusting R13 only.

If adjusting the output voltage of the linear regulators, please pay attention to the recommended resistor value selection guidelines described in the datasheet.

Improving Output Voltage Tolerance

The key to improving the output voltage tolerance is identifying the parameters which affect it, and then taking steps toward improving them.

High dV/dt spikes present in the output voltage waveform under highly dynamic load application (high dI/dt) are due to the ESR and the ESL of the output capacitance. These spikes coincide with the transient load's rising and falling edges, and decreasing their amplitude can be achieved by using lower ESR/ESL output capacitors (such as surface-mount tantalum capacitors), and/or the addition of more ceramic capacitors, which have inherently low ESR/ESL.

The addition of more input-side capacitance and decreasing the input-side capacitor banks' ESR can also help in situations where the input-side ripple is affecting the output regulation. Such an example is excessive ATX 3.3V ripple reducing the collector-to-emitter voltage available for Q3 (2.5V output setting), and thus inducing an output droop component. In such instance, the addition of input-side capacitance and reduction of the ESR component can reduce the output excursion.

Conclusion

The HIP6521EVAL1 evaluation board showcases a highly integrated approach to providing peripheral power control in Pentium 4 computer systems. Sophisticated internal circuits facilitate ACPI implementation with minimum effort and a reduced number of external components.

References

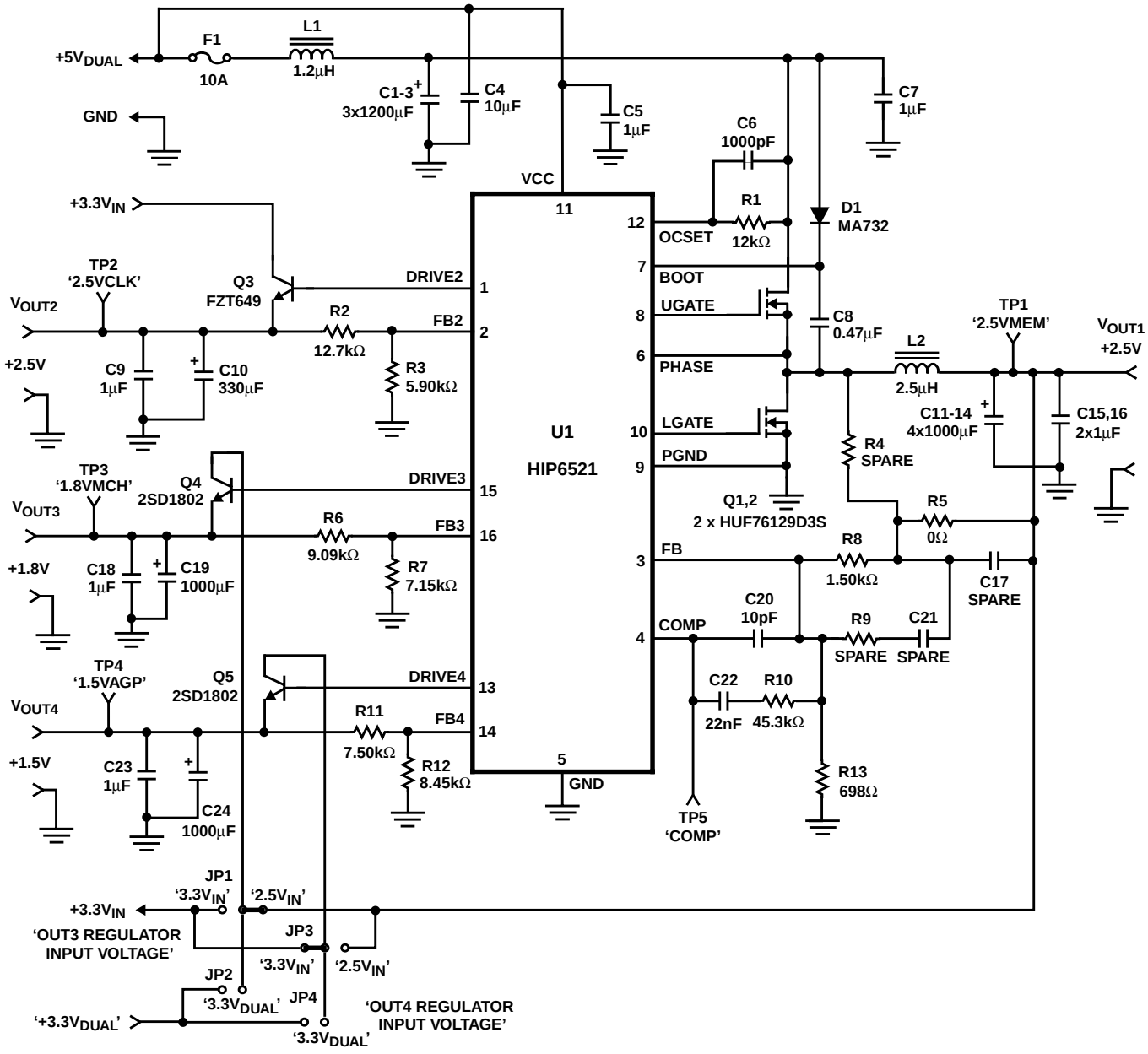
For Intersil documents available on the internet, see web site www.intersil.com/

[1] *HIP6521 Data Sheet,* Intersil Corporation, Power Management Products Division, FN4837, 2000. (www.intersil.com/).

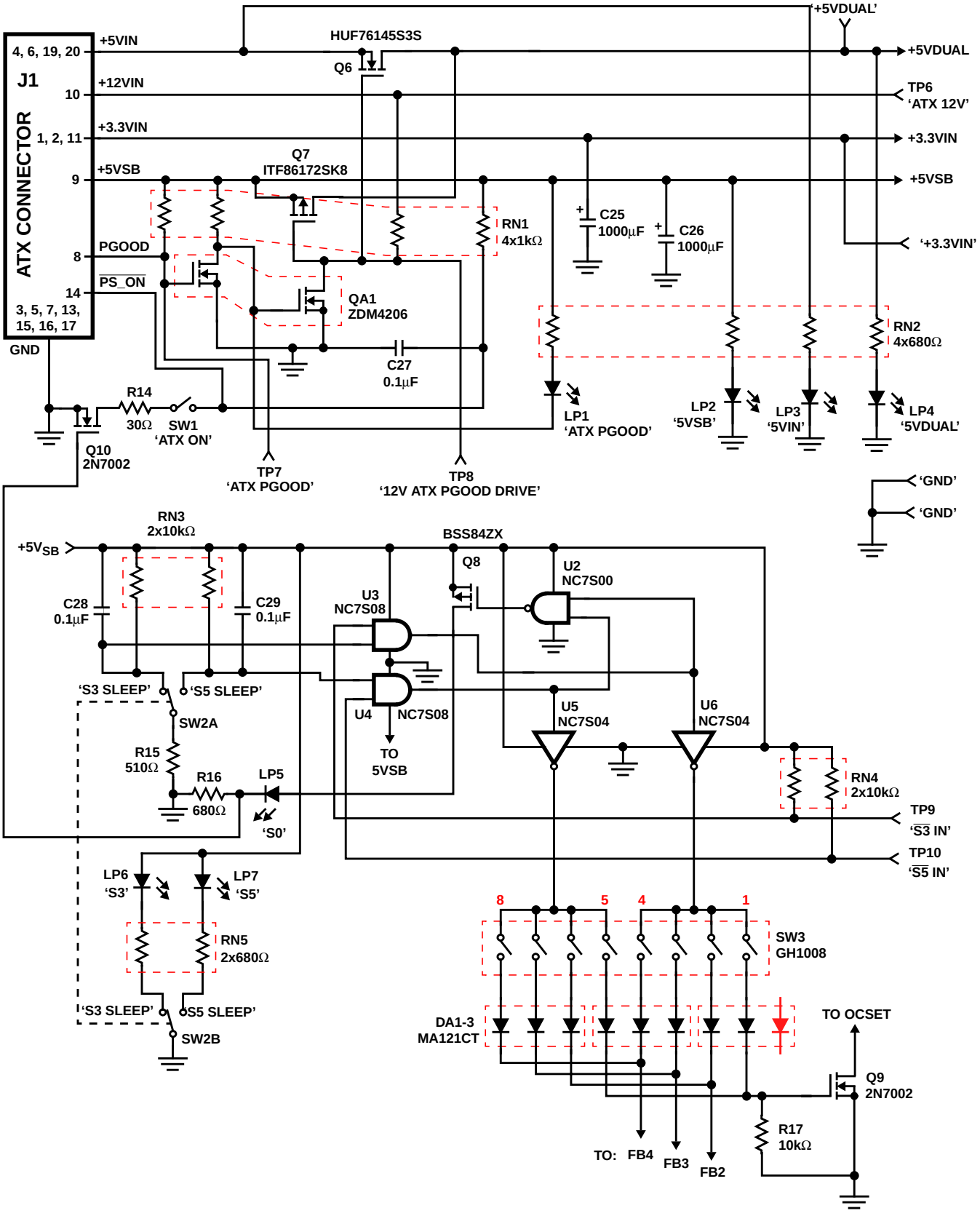
[2] Advanced Configuration and Power Interface (ACPI) Specification, Revision 1.0, December 1996, Intel/Microsoft/Toshiba. (http://www.teleport.com/~acpi/).

[3] ATX Specification, Version 2.02, October 1998, Intel Corporation (http://www.teleport.com/~atx/).

HIP6521EVAL1 Schematic



HIP6521EVAL1 Schematic (Continued)



Bill of Materials for HIP6521EVAL1

REFERENCE	PART NUMBER	DESCRIPTION	PACKAGE	MANUF. OR VENDOR	QTY
C1-3	EEUFC0J122	Al. Electrolytic Capacitor, 6.3V, 1200µF	10 x 16	Panasonic	2
C4	TAJB106M006R	Tantalum Capacitor, 6.3V, 10µF	3.0 x 4.0	AVX	1
C5, 7, 9, 15, 16, 18, 23	1µF Ceramic	Ceramic Capacitor, Y5V, 16V, 1.0µF	0805	Any	7
C6	1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0603	Any	1
C8	0.47µF Ceramic	Ceramic Capacitor, X7R, 16V, 0.47µF	0805	Any	1
C10	6.3ZA330	Al. Electrolytic Capacitor, 6.3V, 330µF	8 x 11.5	Rubycon	1
C11-14, 19, 24	6.3ZA1000	Al. Electrolytic Capacitor, 6.3V, 1000µF	10 x 16	Rubycon	6
C20	10pF Ceramic	Ceramic Capacitor, X7R, 50V	0603	Any	1
C22	22nF Ceramic	Ceramic Capacitor, X7R, 25V	0603	Any	1
C25, 26	6MV1000CA	Al. Electrolytic Capacitor, 6.3V, 1000µF	8 x 11.5	Sanyo	2
C27-29	0603YC104MAT2A	Ceramic Capacitor, X7R, 16V, 0.1µF	0603	AVX	3
C17, 21	Spare		0805		
D1	MA732CT-ND	Schottky Diode, 30V, 30mA	Mini 2P	Digikey	1
DA1-3	MA121CT-ND	Diode Array, 80V, 100mA	Mini 6P	Digikey	3
F1	4182100000	Fuse, 75V, 10A	2.5 x 6.0	Wickmann	1
J1	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		Molex	1
JP1-4	68000-236	Jumper Header	0.1” Spacing	Berg	10/36
	71363-102	Jumper Shunt	0.1” Spacing	Berg	2
L1	1.2µH Inductor	6 Turns of 16AWG onT44-52 Core	8 x 15	Any	1
L2	2.5µH Inductor	8 Turns of 16AWG on T50-52B Core	10 x 17	Any	1
LP1-7	L63111CT-ND	Miniature LED, Through-Board Indicator		Digikey	7
Q1,2	HUF76129D3S	UltraFET™ MOSFET, 30V, 16mΩ	TO-252AA	Intersil	2
Q3	FZT649	NPN Bipolar, 25V, 3A	SOT-223	Zetex	1
Q4,5	2SD1802	NPN Bipolar, 50V, 3A	TO-252AA	Sanyo	2
Q6	HUF76145S3S	UltraFET™ MOSFET, 30V, 5.5mΩ	TO-263	Intersil	1
Q7	ITF86172SK8T	TrenchFET MOSFET, 30V, 23mΩ	SO-8	Intersil	1
Q8	BSS84ZXCT-ND	Logic P-MOSFET, 50V, 10Ω	SOT-23	Digikey	1
Q9, 10	2N7002	Logic N-MOSFET, 25V, 5Ω	SOT-23	Any	2
QA1	ZDM4206NCT-ND	Small-Signal Dual MOSFET, 60V, 1Ω	SM-8	Digikey	1
R1	12kΩ	Resistor, 5%, 0.1W	0603	Any	1
R2	12.7kΩ	Resistor, 1%, 0.1W	0603	Any	1
R3	5.90kΩ	Resistor, 1%, 0.1W	0603	Any	1
R5	0Ω	Shorting Resistor	0603	Any	1
R6	9.09kΩ	Resistor, 1%, 0.1W	0603	Any	1
R7	7.15kΩ	Resistor, 1%, 0.1W	0603	Any	1
R8	1.50kΩ	Resistor, 1%, 0.1W	0603	Any	1
R10	45.3kΩ	Resistor, 1%, 0.1W	0603	Any	1
R11	7.50kΩ	Resistor, 1%, 0.1W	0603	Any	1
R12	8.45kΩ	Resistor, 1%, 0.1W	0603	Any	1
R13	698Ω	Resistor, 1%, 0.1W	0603	Any	1
R14	30Ω	Resistor, 5%, 0.1W	0603	Any	1
R15	510Ω	Resistor, 5%, 0.1W	0603	Any	1
R16	680Ω	Resistor, 5%, 0.1W	0603	Any	1
R17	10kΩ	Resistor, 5%, 0.1W	0603	Any	1
R4,9	Spare		0603		
RN1	Y9102CT-ND	4-Resistor Network, 1.0kΩ, 5%, 0.1W	3.2 x 1.6	Digikey	1

Bill of Materials for HIP6521EVAL1

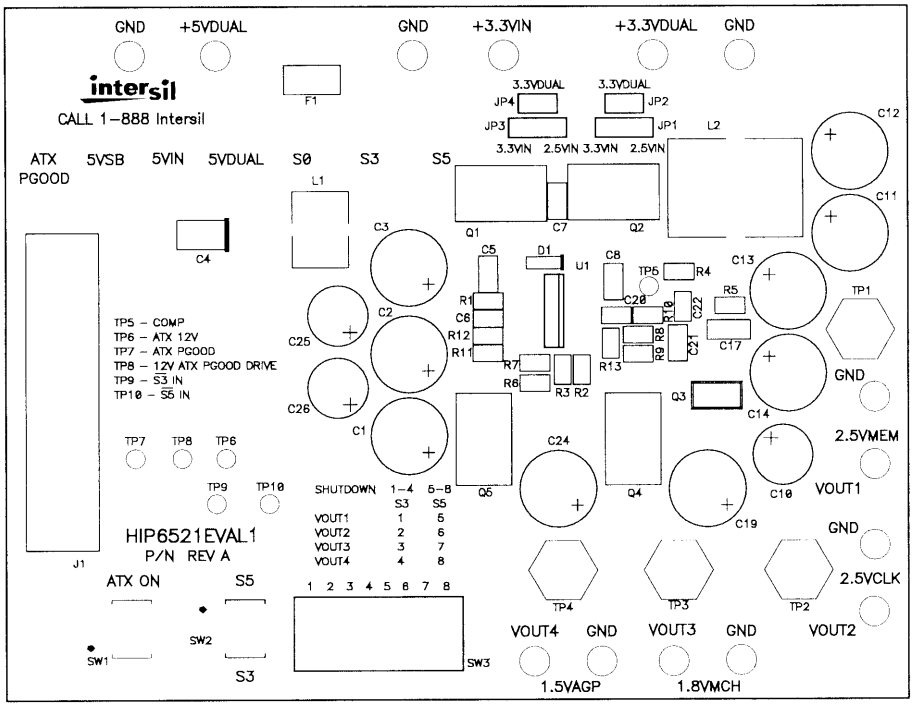
REFERENCE	PART NUMBER	DESCRIPTION	PACKAGE	MANUF. OR VENDOR	QTY
RN2	Y9681CT-ND	4-Resistor Network, 680Ω, 5%, 0.1W	3.2 x 1.6	Digikey	1
RN3,4	Y8103CT-ND	2-Resistor Network, 10kΩ, 5%, 0.1W	1.6 x 1.6	Digikey	2
RN5	Y8681CT-ND	2-Resistor Network, 680Ω, 5%, 0.1W	1.6 x 1.6	Digikey	1
SW1	GT12MSCKE	Miniature Switch, Single Pole, Single Throw		C&K	1
SW2	GT23MSCKE	Miniature Switch, Double Pole, Double Throw, On-Off-On		C&K	1
SW3	GH1008-ND	Miniature Rocker Switch, 8-Pole, Single Throw		Digikey	1
TP1-4	1314353-00	Test Point, Scope Probe		Tektronics	4
TP5-10	SPCJ-123-01	Test Point		Jolo	6
U1	HIP6521CB	Synchronous Switcher and Triple Linear Controller	SOIC-16	Intersil	1
U2	NC7S00	2-Input NAND Gate	5-Pin SOT-23	Fairchild	1
U3, 4	NC7S08	2-Input AND Gate	5-Pin SOT-23	Fairchild	2
U5, 6	NC7S04	CMOS Inverter	5-Pin SOT-23	Fairchild	2
$+3.3V_{DUAL}$, $+3.3V_{IN}$, $+5V_{DUAL}$, $+V_{OUT1}$, $+V_{OUT2}$, $+V_{OUT3}$, $+V_{OUT4}$, GND	1514-2	Terminal Post		Keystone	14

NOTE:

1. Mount SW1 such that the side with the part marking faces the white dot in the solder mask.

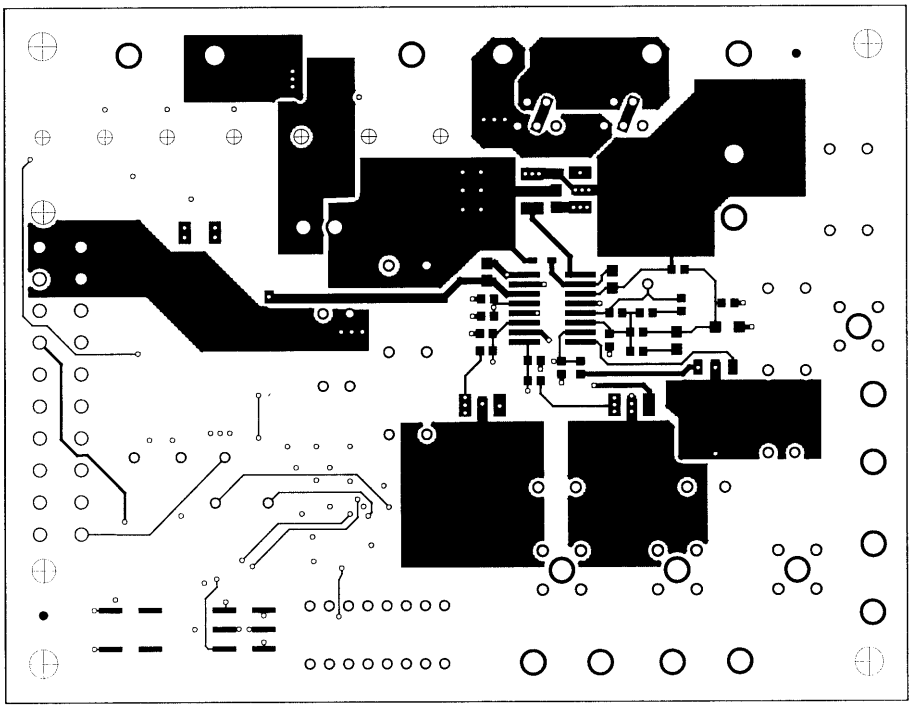
HIP6521EVAL1 Layout

TOP SILK SCREEN

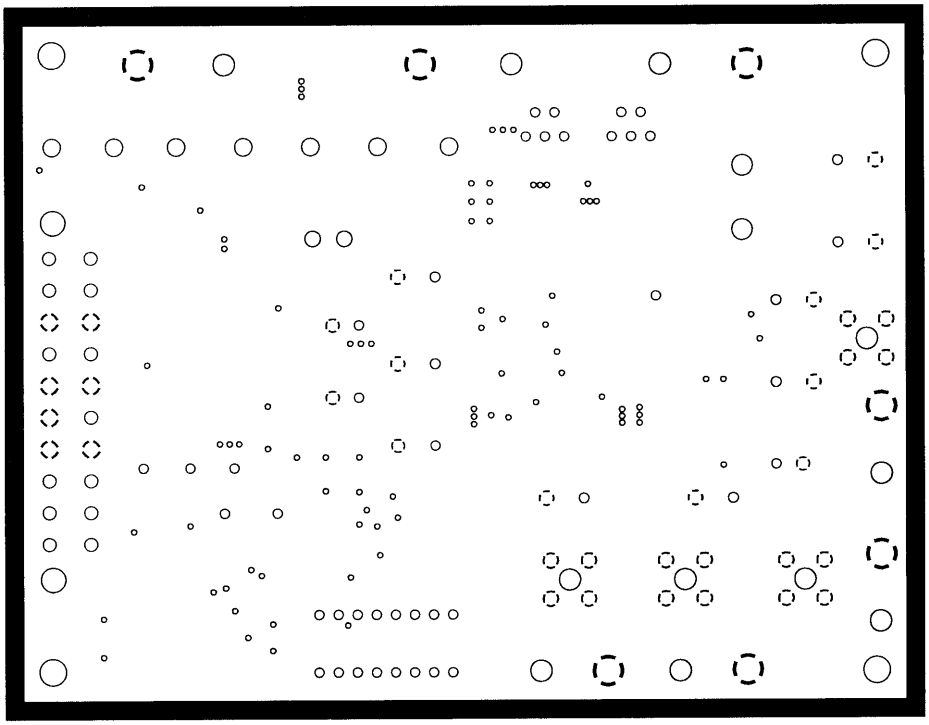


HIP6521EVAL1 Layout (Continued)

TOP LAYER

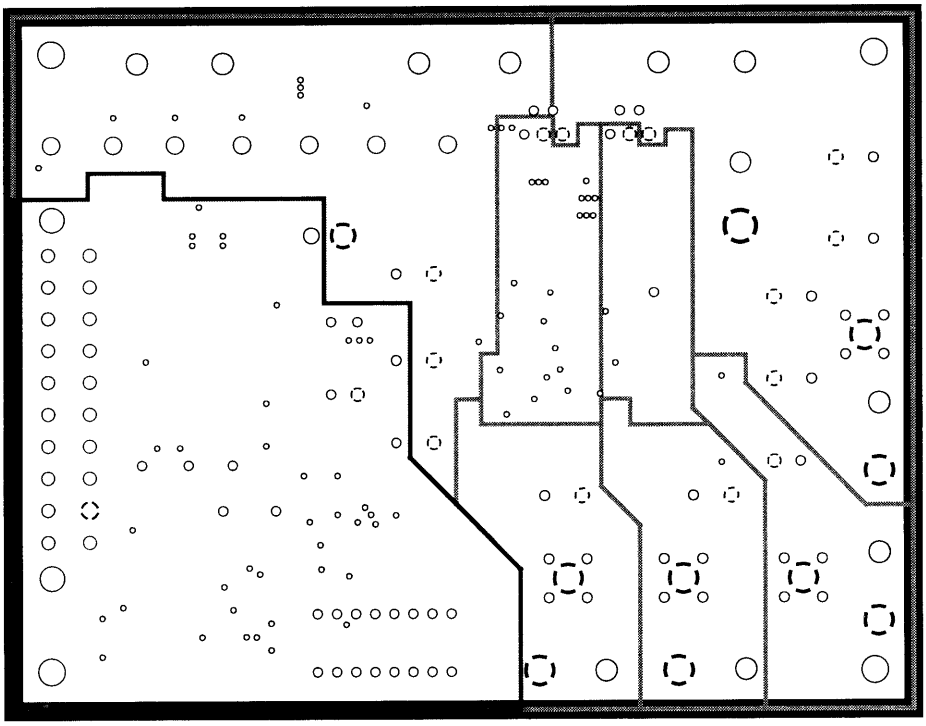


GROUND LAYER

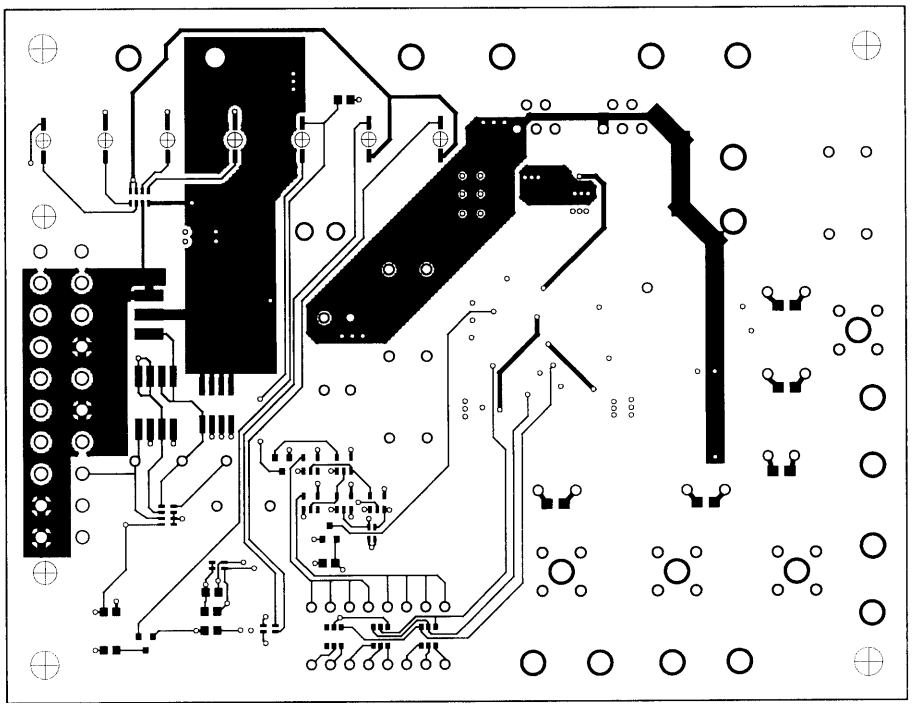


HIP6521EVAL1 Layout (Continued)

POWER LAYER

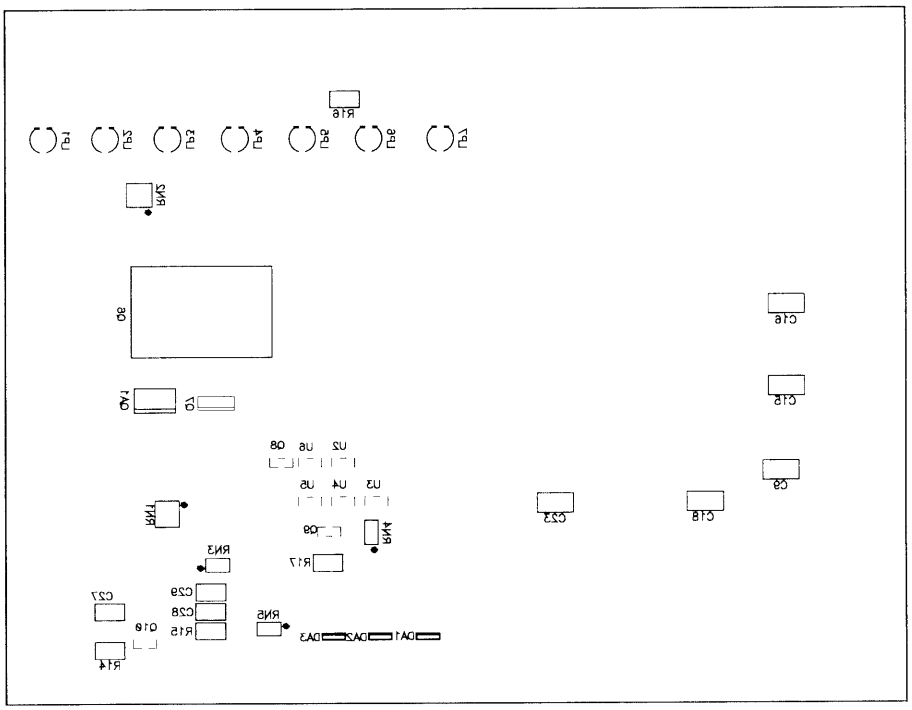


BOTTOM LAYER



HIP6521EVAL1 Layout (Continued)

BOTTOM SILK SCREEN



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